3V to 5.5V, 50Mbps Full Duplex RS485 Transceivers

GENERAL DESCRIPTION

SiLM1452L is a noise-immune, full duplex RS485/RS422 transceiver designed to operate in rugged industrial environments. The bus pins of the device are robust to high levels of electrostatic discharge (ESD) events. The fail-safe circuitry guarantees a logic high receiver output when the receiver inputs are open or short.

The SiLM1452L operates from a single supply between 3 V and 5.5 V. It features an extended common-mode voltage range which makes it suitable for multi-point applications over long cable runs.

The SiLM1452L is available in MSOP10 package for space constrained applications and it supports ambient temperatures from –40°C to 125°C.

APPLICATION

- Motor driver
- Factory automation and control
- Grid infrastructure
- Building automation
- HVAC systems
- Video surveillance
- Process analytics

FEATURES

- Meets or exceeds the requirements of the TIA/EIA-485 standard
- 50Mbps data rates, full duplex
- 3V to 5.5V supply voltage
- Differential output exceeds 2.1V for PROFIBUS compatibility with 5V supply
- Extended operational common mode range: ±15V
- Large receiver hysteresis for noise rejection
- Low power consumption
  - Standby supply current: <1uA
  - Current during operation: <2mA
- Ambient temperature: –40°C to 125°C
- Glitch free power up/down for hot plug-in capability
- Open, short and idle bus failsafe
- 1/8 unit load (up to 256 bus nodes)

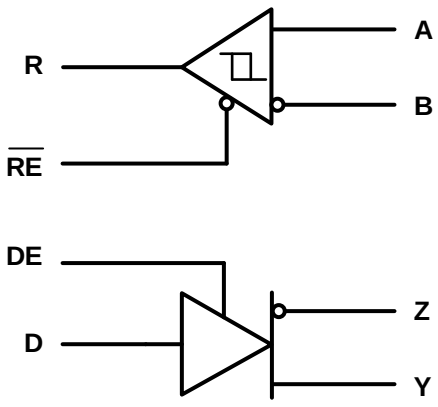

Figure 1. SiLM1452L simplified schematic

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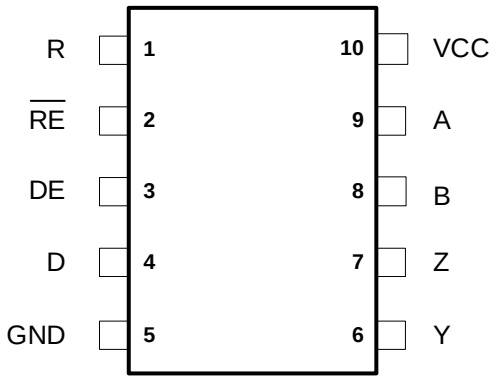
PIN CONFIGURATION

Package	Pin Configuration (Top View)
MSOP10	

PIN DESCRIPTION

No.	Pin Name	Description
1	R	Receive data output
2	$\overline{RE}$	Receiver enable, active low, internal pull up.
3	DE	Driver enable, active high, internal pull down
4	D	Driver data input
5	GND	Device ground
6	Y	Digital bus output, Y (complementary to Z)
7	Z	Digital bus output, Z (complementary to Y)
8	B	Bus I/O port, B (complementary to A)
9	A	Bus I/O port, A (complementary to B)
10	VCC	Power supply

FUNCTIONAL BLOCK DIAGRAM

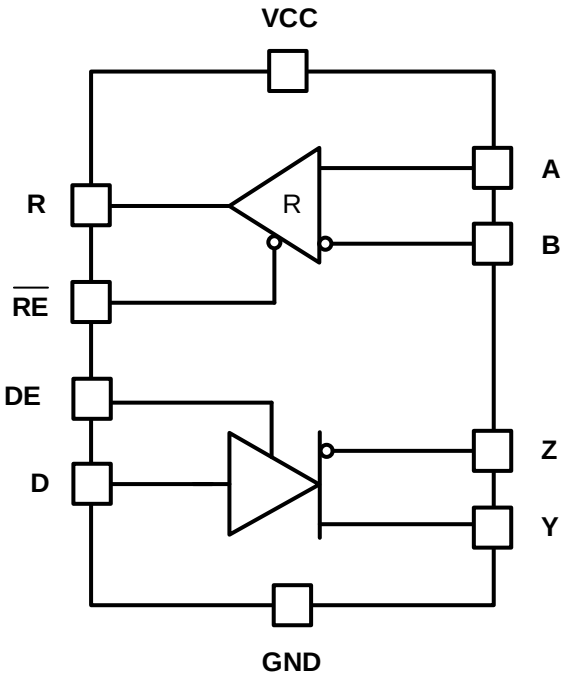


Figure 2. SiLM1452L Block Diagram

ORDERING INFORMATION

Order Part No.	Package	QTY
SiLM1452LGC-DG	MSOP10, Pb-Free	4000/Reel

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Units
V_{CC}	Supply Voltage	-0.3	6	V
V_I	Voltage range at any bus pin (A, B, Y or Z) as differential or common mode with respect to GND	-18	18	V
V_{IN}	Voltage at any logic pin (D, DE or $\overline{RE}$)	-0.3	6	V
I_{OR}	Receiver output current	-24	24	mA
T_J	Junction Temperature	-55	150	°C
T_S	Storage Temperature	-65	150	

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min	Max	Units
V_{CC}	Supply Voltage	3	5.5	V
V_I	Input voltage at any bus terminal	-15	15	V
V_{ID}	Differential input voltage	-15	15	V
V_{IH}	High level input voltage (D, DE or $\overline{RE}$)	2	V_{CC}	V
V_{IL}	Low level input voltage (D, DE or $\overline{RE}$)	0	0.8	V
I_O	Driver output current	-60	60	mA
I_{OR}	Receiver output current	-8	8	mA
R_L	Differential load resistance	54		Ω
$1/t_{UI}$	Signaling rate		50	Mbps
T_J	Junction Temperature	-40	150	°C
T_A	Ambient Temperature	-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V_{ESD}	HBM: Bus pins to GND	±15	kV
	HBM: All other pins	±3.5	kV
	CDM	±2	kV

ELECTRICAL CHARACTERISTICS (DC)

All typical values at V_{CC} = 5V and T_A = 25°C, all min and max specifications are at recommended operating conditions and T_J = -40°C to 125°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Driver						
$\|V_{OD1}\|$	Driver differential output voltage	R_L=60Ω, -15V ≤ V_{TEST} ≤ 15V, see Figure 3	1.5	3		V
$\|V_{OD2}\|$		R_L=60Ω, -15V ≤ V_{TEST} ≤ 15V, 4.5V ≤ V_{CC} ≤ 5.5V, see Figure 3	2.1	3		V
$\|V_{OD3}\|$		R_L=100Ω, see Figure 4	1.8	3.6		V
$\|V_{OD4}\|$		R_L=54Ω, see Figure 4	1.5	3.1		V
$\Delta\|V_{OD}\|$	Change in differential output voltage	R_L=54Ω, see Figure 4	-100		100	mV
V_{OC}	Common mode output voltage		1	V_{CC}/2	3	V
ΔVOC(SS)	Change in steady state common mode output voltage		-100		100	mV
I_{OS}	Short circuit output current	DE=VCC, -7V ≤ V_O ≤ 12V	-250		250	mA
Receiver						
I_{I1}	Bus input current	DE=0V, VCC=0V or 5.5V, V_I=12V		75	125	uA
I_{I2}		DE=0V, VCC=0V or 5.5V, V_I= -7V	-100	-70		uA
I_{I3}		DE=0V, VCC=0V or 5.5V, V_I=15V		95	125	uA
I_{I4}		DE=0V, VCC=0V or 5.5V, V_I= -15V	-200	-120		uA
V_{TH+}	Positive going input threshold voltage	Over common mode range of ±15V		-105	-20	mV
V_{TH-}	Negative going input threshold voltage		-200	-130		mV
V_{HYS}	Input hysteresis			25		mV
V_{OH}	Output high voltage	I_{OH} = -8mA	V_{CC}-0.4	V_{CC}-0.2		V
V_{OL}	Output low voltage	I_{OH} = 8mA		0.2	0.4	V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OZR}	Output high impedance current	V_O=0V or V_{CC}, $\overline{RE}$ =V_{CC}	-1		1	uA
Logic						
I_{IN}	Input current (D, DE, $\overline{RE}$)	3V ≤ V_{CC} ≤ 5.5V, 0V ≤ V_{IN} ≤ V_{CC}	-6		6	uA
Supply Current						
I_{CC1}	Supply current with driver and receiver enabled	$\overline{RE}$ =0V, DE=V_{CC}, No load		1.5	2	mA
I_{CC2}	Supply current with driver enabled and receiver disabled	$\overline{RE}$ =V_{CC}, DE=V_{CC}, No load		1.35	1.8	mA
I_{CC3}	Supply current with driver disabled and receiver enabled	$\overline{RE}$ =0V, DE=0V, No load		480	700	uA
I_{CC4}	Supply current with driver and receiver disabled	$\overline{RE}$ =V_{CC}, DE=0V, D=open, No load		0.1	1	uA
Thermal Protection						
T_{TSD}	Thermal Shutdown Temperature			170		°C
T_{HYS}	Thermal Shutdown Hysteresis			15		°C

SWITCHING CHARACTERISTICS (AC)

All typical values at V_{CC} = 5V and T_A = 25°C, all min and max specifications are at recommended operating conditions and T_J = -40°C to 125°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Driver						
t_r, t_f	Differential output rise/fall time	R_L=54Ω, C_L=50pF, see Figure 5		2	8	ns
t_{PHL}, t_{PLH}	Propagation delay			10	20	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL}-t_{PLH}\|$				6	ns
t_{PHZ}, t_{PLZ}	Disable time			10	20	ns
t_{PZH}, t_{PZL}	Enable time	$\overline{RE}$ =0V, see Figure 6 and Figure 7		10	25	ns
		$\overline{RE}$ =V_{CC}, see Figure 6 and Figure 7		8	15	us

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Receiver						
t_r, t_f	Output rise/fall time	C_L=15pF, see Figure 8		2	6	ns
t_{PHL}, t_{PLH}	Propagation delay			20	35	ns
$t_{SK(P)}$	Pulse skew, $\|t_{PHL}-t_{PLH}\|$				7	ns
t_{PHZ}, t_{PLZ}	Disable time			8	15	ns
t_{PZH1}, t_{PZL1}, t_{PZH2}, t_{PZL2}	Enable time	DE=V_{CC}, see Figure 9		8	15	ns
		DE=0V, see Figure 10		9	15	us

PARAMETER MEASUREMENT INFORMATION

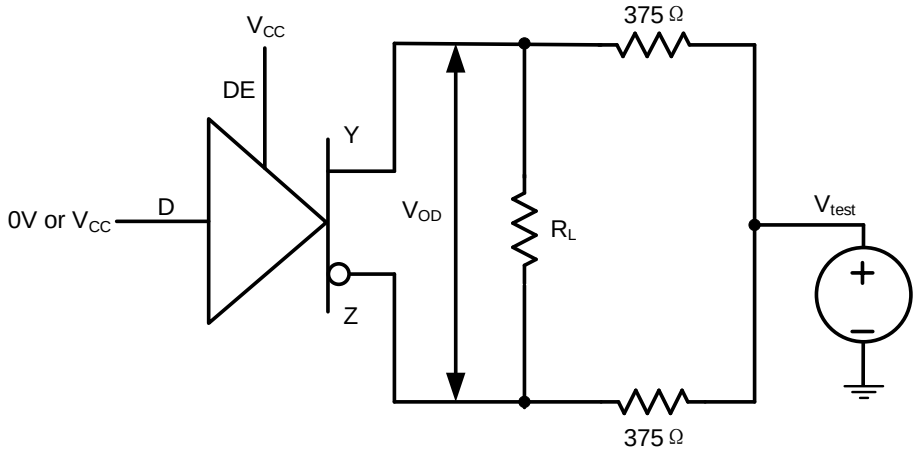


Figure 3. Measurement of driver differential output voltage with common mode load

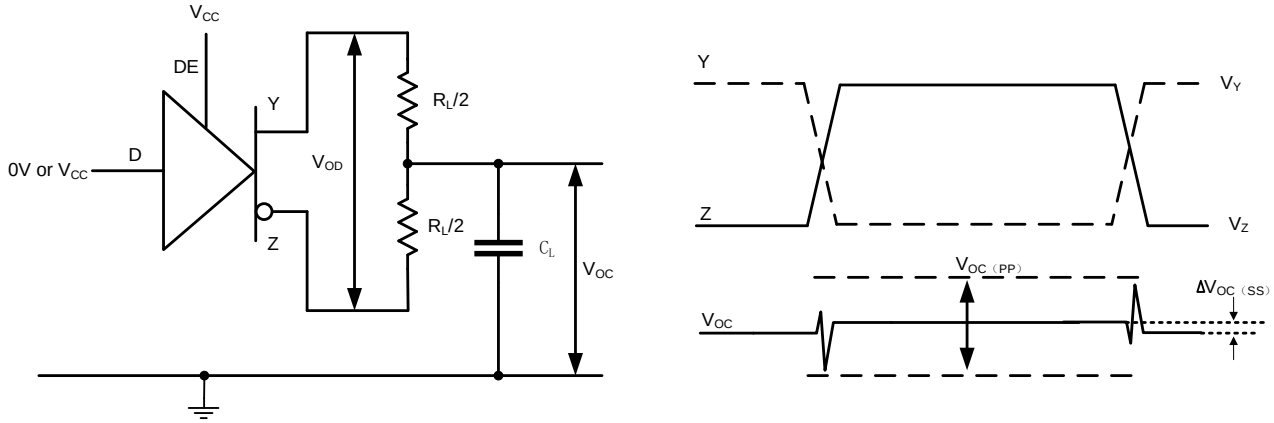


Figure 4. Measurement of driver differential and common mode output with RS485 Load

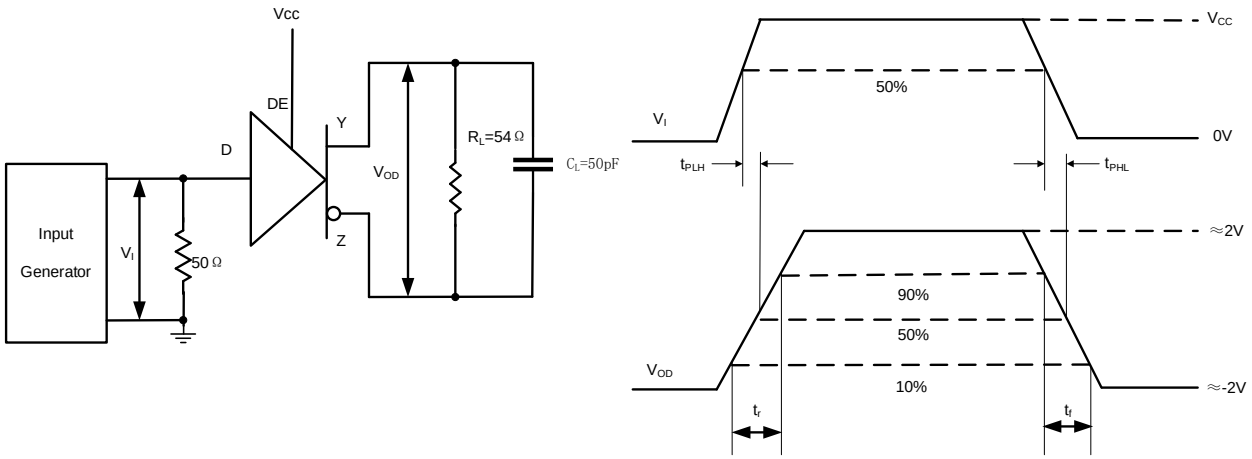


Figure 5. Measurement of driver differential output rise and fall times and propagation delays

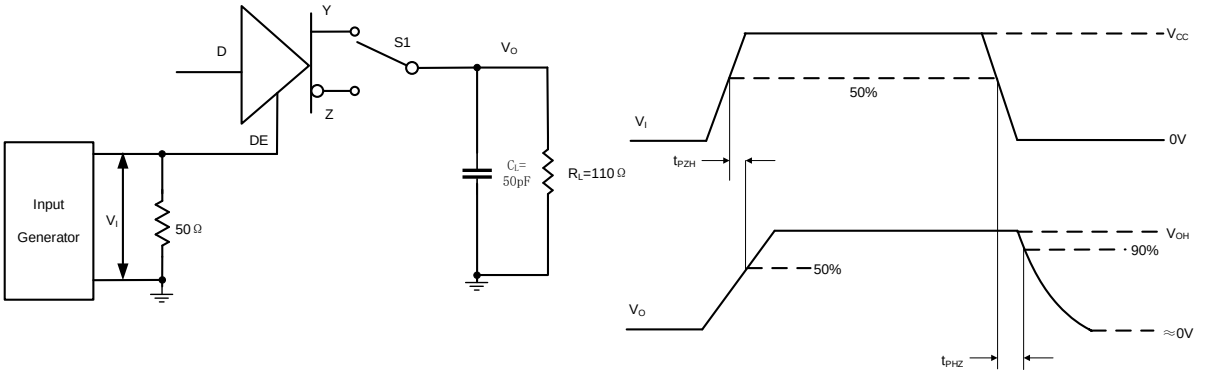


Figure 6. Measurement of driver enable and disable times with active high output and pull-down load

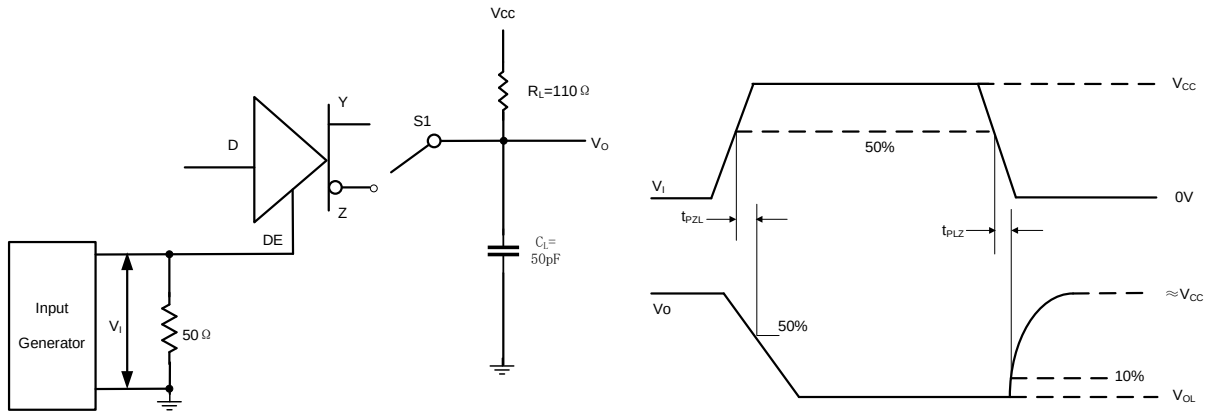


Figure 7. Measurement of driver enable and disable times with active low output and pull-up load

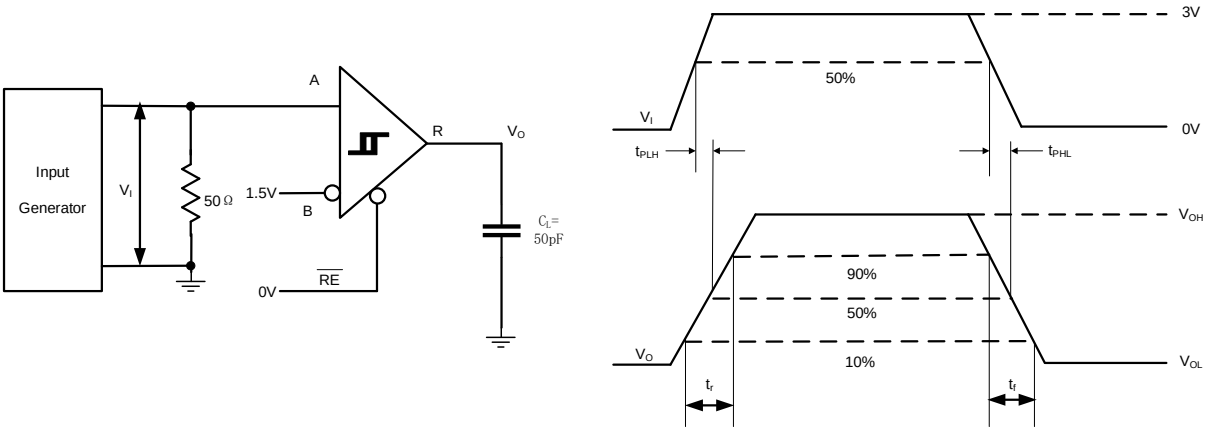


Figure 8. Measurement of receiver output rise and fall times and propagation delays

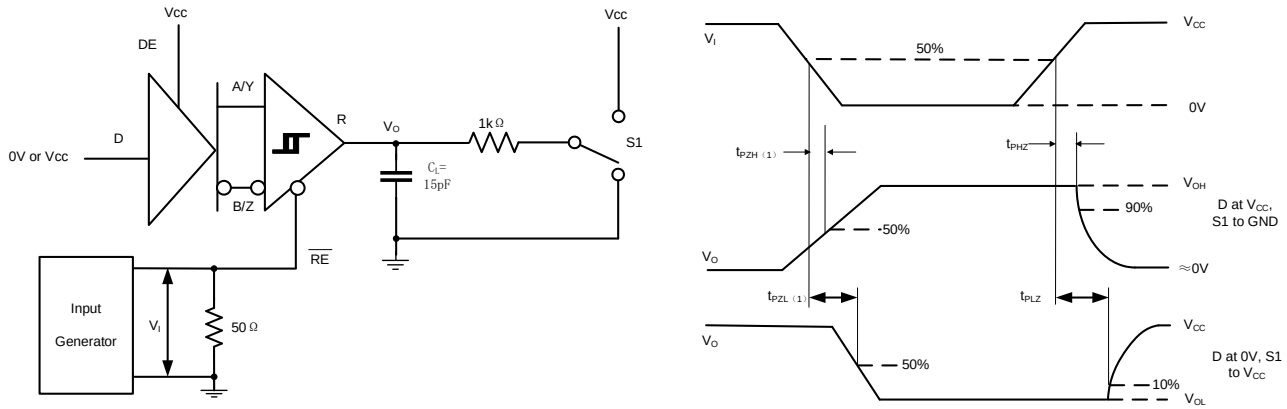


Figure 9. Measurement of receiver enable/disable times with driver enabled

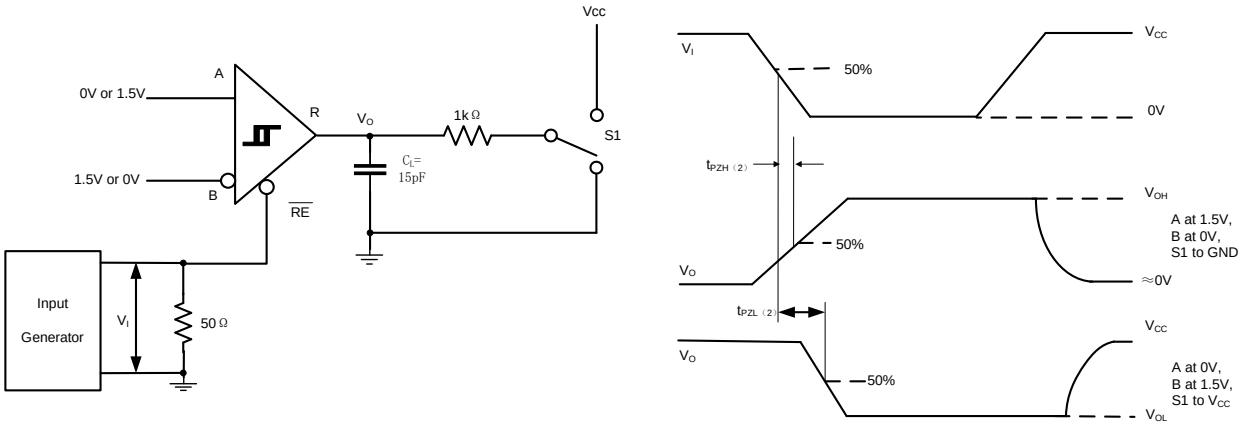


Figure 10. Measurement of receiver enable times with driver disabled

FEATURE DESCRIPTION

SiLM1452L is a full duplex RS-485 transceiver with data transmission up to 50 Mbps. It has active-high driver enable and active low receiver enable. A standby current of less than 1 μA can be achieved by disabling both driver and receiver. The SiLM1452L has a higher typical differential output voltage (V_{OD}) than traditional transceivers for better noise immunity. A minimum differential output voltage of 2.1 V is specified with V_{CC} voltage of 5 V ±10% to meet the requirements of PROFIBUS applications.

The SiLM1452L provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. The receiver output remains logic high under a bus-idle or bus-short conditions without the need for external failsafe biasing resistors. Device operation is specified over a wide ambient temperature range from –40°C to 125°C.

Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs Y and Z follow the logic states at data input D. A logic high at D causes Y to turn high and Z to turn low. In this case the differential output voltage defined as $V_{OD} = V_Y – V_Z$ is positive. When D is low, the output states reverse: Z turns high, Y becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to VCC, thus, when left open while the driver is enabled, output Y turns high and Z turns low.

Table 1. Driver function table for SiLM1452L

Input	Enable	Outputs		Function
D	DE	Y	Z	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	Open	Z	Z	Driver disabled by default
Open	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A – V_B$ is higher than the positive input threshold, V_{TH+}, the receiver output, R, turns high. When V_{ID} is lower than the negative input threshold, V_{TH-}, the receiver output, R, turns low. If V_{ID} is between V_{TH+} and V_{TH-} the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver function table for SiLM1452L

Differential Input	Enable	Output	Function
$V_{ID}=V_A-V_B$	$\overline{RE}$	R	
$V_{TH+}<V_{ID}$	L	H	Receive valid bus high
$V_{TH-}<V_{ID}<V_{TH+}$	L	unknow	Indeterminate bus state
$V_{ID}<V_{TH-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled

X	Open	Z	Receiver disabled by default
Open circuit bus	L	H	Fail-safe high output
Short circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

Receiver Failsafe

The differential receiver of the SiLM1452L is failsafe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input indeterminate range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{TH+}, V_{TH-}, and V_{HYS} (the separation between V_{TH+} and V_{TH-}). As shown in the Electrical Characteristics (DC) table, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{TH+} threshold, and the receiver output will be high. Only when the differential input is more than V_{HYS} below V_{TH+} will the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{TH+}.

TYPICAL APPLICATION

The SiLM1452L is a full-duplex RS-485 transceivers. It requires two signal pairs (four wires), and allows each node to transmit data on one pair while simultaneously receiving data on the other pair.

RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable as shown in Figure 11. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, generally allows for higher data rates over longer cable length.

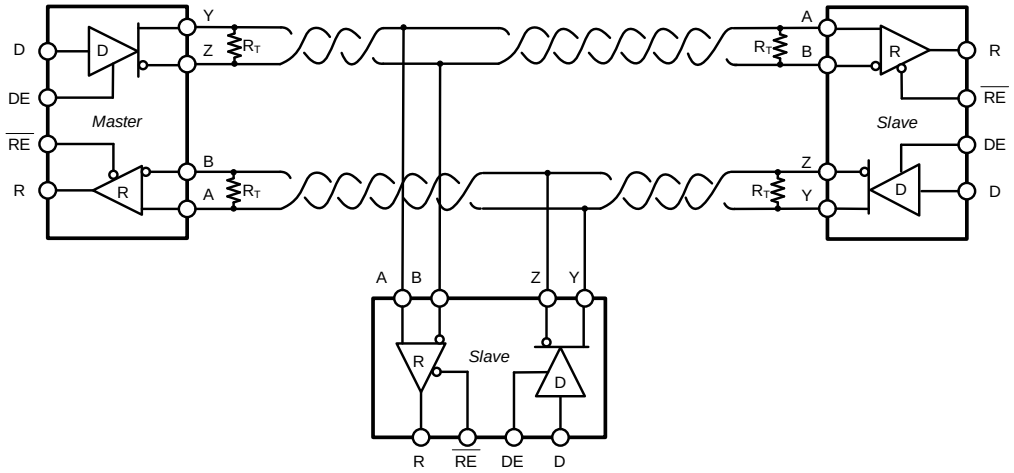
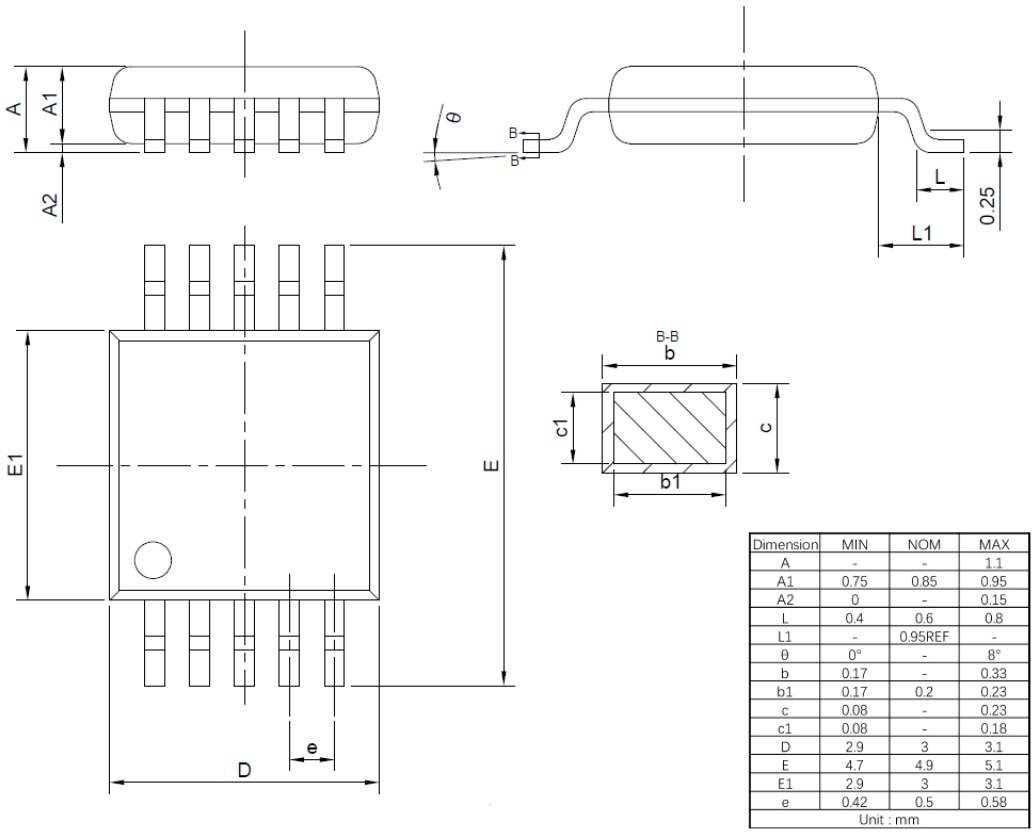


Figure 11. Typical RS-485 Network with Full-Duplex Transceivers

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	1.1
A1	0.75	0.85	0.95
A2	0	-	0.15
L	0.4	0.6	0.8
L1	-	0.95REF	-
θ	0°	-	8°
b	0.17	-	0.33
b1	0.17	0.2	0.23
c	0.08	-	0.23
c1	0.08	-	0.18
D	2.9	3	3.1
E	4.7	4.9	5.1
E1	2.9	3	3.1
e	0.42	0.5	0.58
Unit : mm			

Figure 12. MSOP10 Package Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: 2025-03-04	
Whole document	Rev1.0 datasheet release