

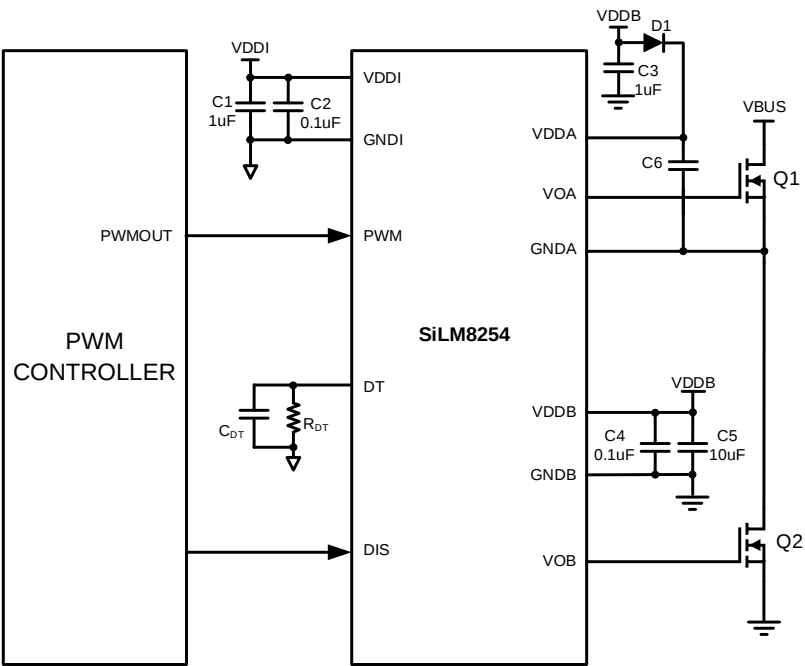


Figure 2. SiLM8254 Application Circuit

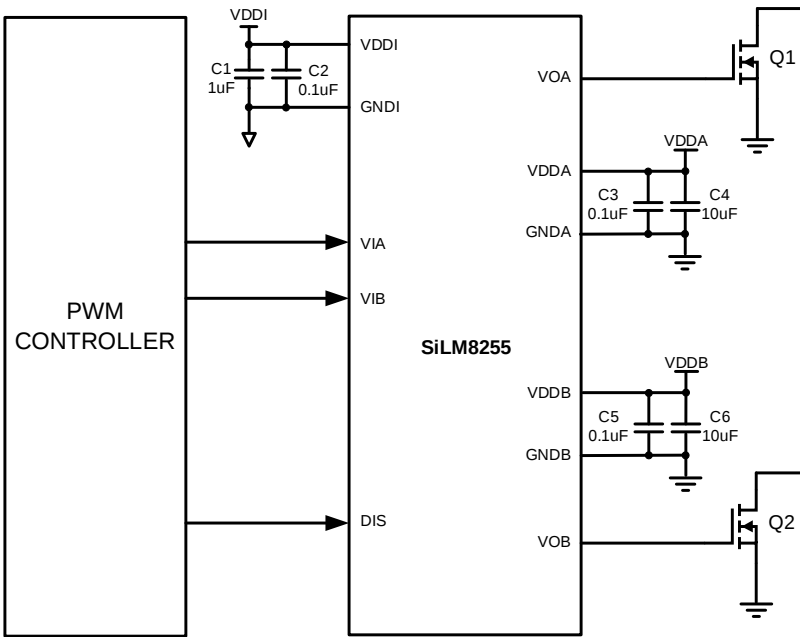
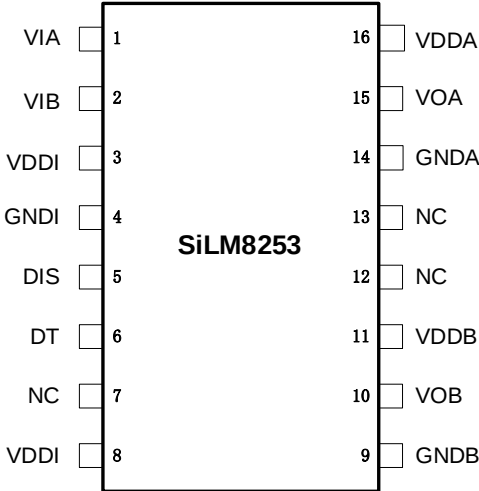
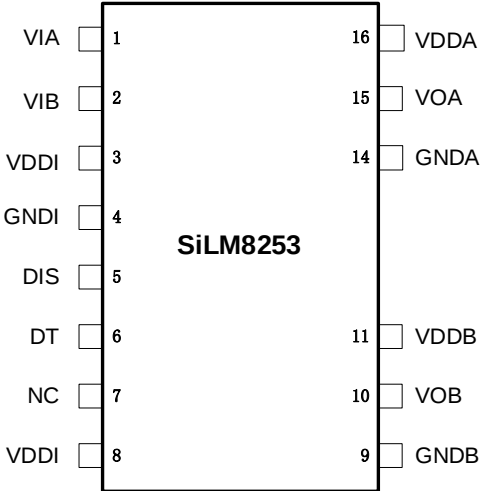
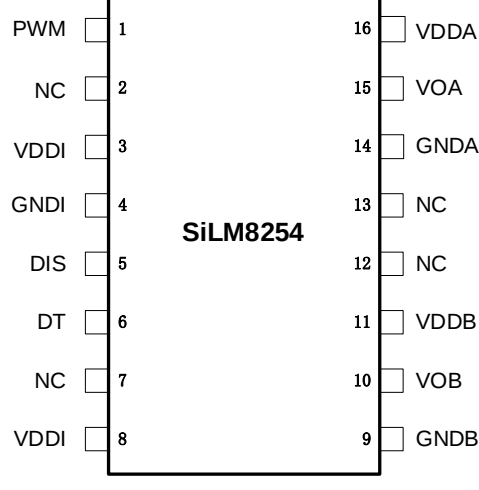
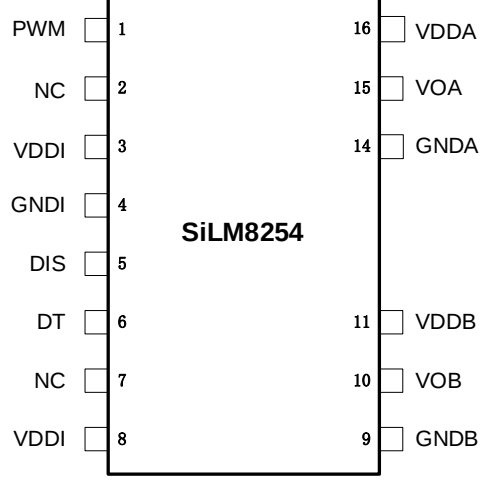
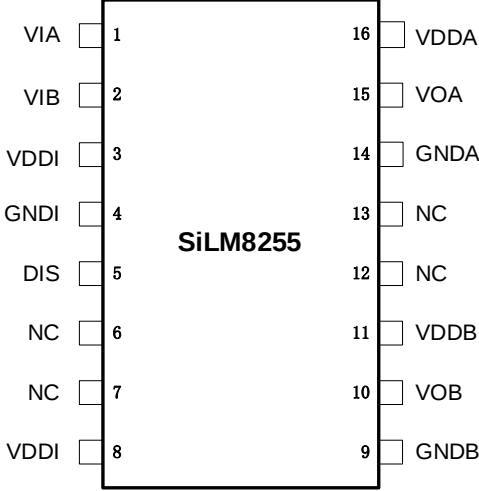
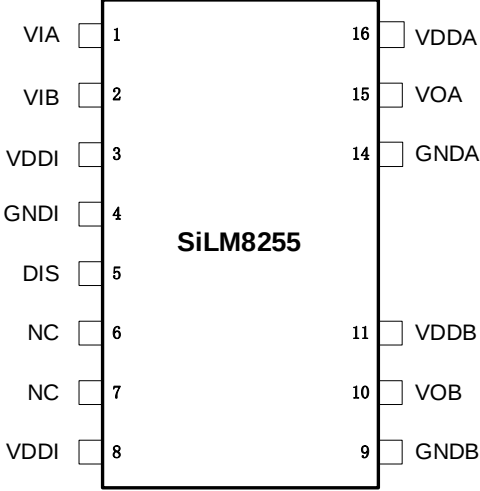


Figure 3. SiLM8255 Application Circuit

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PIN CONFIGURATION

Part Number	Pin Configuration (Top View)	
	SOP16/SOP16W	SOP14W
SiLM8253		
SiLM8254		
SiLM8255		

PIN DESCRIPTION

Table 1. SiLM8253 Pin Description

No.	Pin	Description
1	VIA	Input of driver A. The output of driver A is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
2	VIB	Input of driver B. The output of driver B is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
3	VDDI	Input power supply. A local low ESR and ESL capacitor should be connected between VDDI and GNDI.
4	GNDI	Input power ground.
5	DIS	Device disable input. When DIS pin is high, both driver is disabled and driver output is low. When DIS pin is low, it allows the device to perform in normal operation.
6	DT	Dead time programming input. Connect a resistor between DT and GNDI to program the dead time. A bypassing capacitor, 2.2nF or greater, is recommended to be put between DT and GNDI to achieve better noise immunity.
7	NC	No connection
8	VDDI	Input power supply. This pin is internally connected to pin3.
9	GNDB	Power ground of driver B.
10	VOB	Output of driver B.
11	VDDDB	Power supply of driver B. A local low ESR and ESL capacitor should be connected between VDDDB and GNDB.
12	NC	No connection. Pin12 is removed in SOP14W.
13	NC	No connection. Pin13 is removed in SOP14W.
14	GNDA	Power ground of driver A.
15	VOA	Output of driver A.
16	VDDA	Power supply of driver A. A local low ESR and ESL capacitor should be connected between VDDA and GNDA.

Table 2. SiLM8254 Pin Description

No.	Pin	Description
1	PWM	PWM input. The output of driver A is in phase with PWM input and the output of driver B is out of phase with PWM input.
2	NC	No connection
3	VDDI	Input power supply. A local low ESR and ESL capacitor should be connected between VDDI and GNDI.
4	GNDI	Input power ground.
5	DIS	Device disable input. When DIS pin is high, both driver is disabled and driver output is low. When DIS pin is low, it allows the device to perform in normal operation.
6	DT	Dead time programming input. Connect a resistor between DT and GNDI to program the dead time. A bypassing capacitor, 2.2nF or greater, is recommended to be put between DT and GNDI to achieve better noise immunity.

No.	Pin	Description
7	NC	No connection
8	VDDI	Input power supply. This pin is internally connected to pin3.
9	GNDB	Power ground of driver B.
10	VOB	Output of driver B.
11	VDDDB	Power supply of driver B. A local low ESR and ESL capacitor should be connected between VDDDB and GNDB.
12	NC	No connection. Pin12 is removed in SOP14W.
13	NC	No connection. Pin13 is removed in SOP14W.
14	GNDA	Power ground of driver A.
15	VOA	Output of driver A.
16	VDDA	Power supply of driver A. A local low ESR and ESL capacitor should be connected between VDDA and GNDA.

Table 3. SiLM8255 Pin Description

No.	Pin	Description
1	VIA	Input of driver A. The output of driver A is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
2	VIB	Input of driver B. The output of driver B is in phase with the input. This pin is pulled low internally if left open. Recommend to connect this pin to ground if not used for better noise immunity.
3	VDDI	Input power supply. A local low ESR and ESL capacitor should be connected between VDDI and GNDI.
4	GNDI	Input power ground.
5	DIS	Device disable input. When DIS pin is high, both driver is disabled and driver output is low. When DIS pin is low, it allows the device to perform in normal operation.
6	NC	No connection
7	NC	No connection
8	VDDI	Input power supply. This pin is internally connected to pin3.
9	GNDB	Power ground of driver B.
10	VOB	Output of driver B.
11	VDDDB	Power supply of driver B. A local low ESR and ESL capacitor should be connected between VDDDB and GNDB.
12	NC	No connection. Pin12 is removed in SOP14W.
13	NC	No connection. Pin13 is removed in SOP14W.
14	GNDA	Power ground of driver A.
15	VOA	Output of driver A.
16	VDDA	Power supply of driver A. A local low ESR and ESL capacitor should be connected between VDDA and GNDA.

FUNCTIONAL BLOCK DIAGRAM

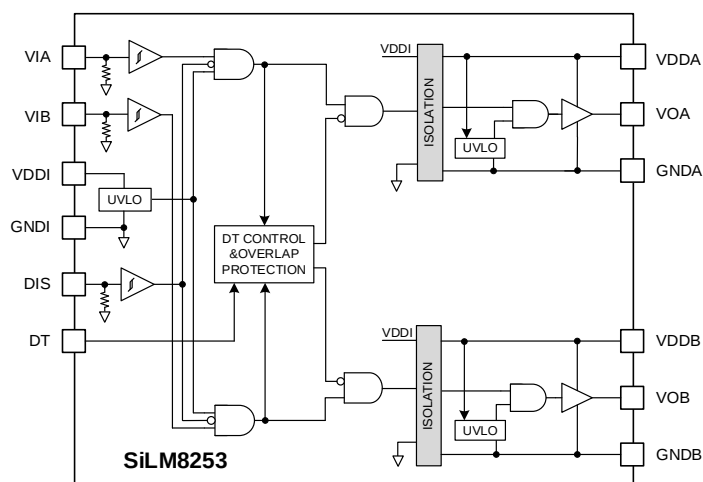


Figure 4. SiLM8253 Functional Block Diagram

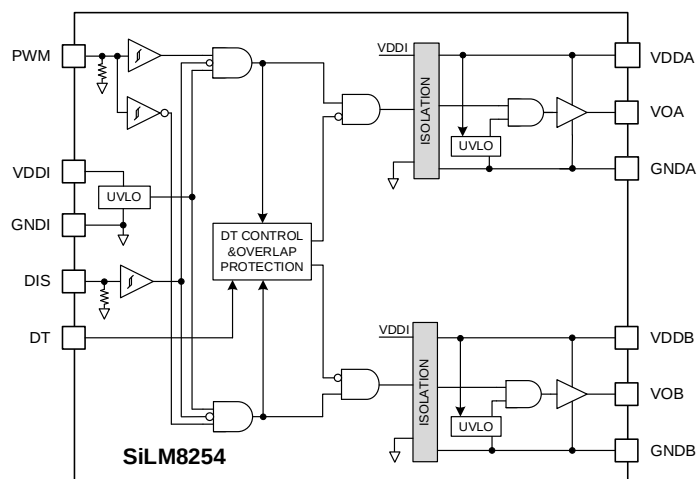


Figure 5. SiLM8254 Functional Block Diagram

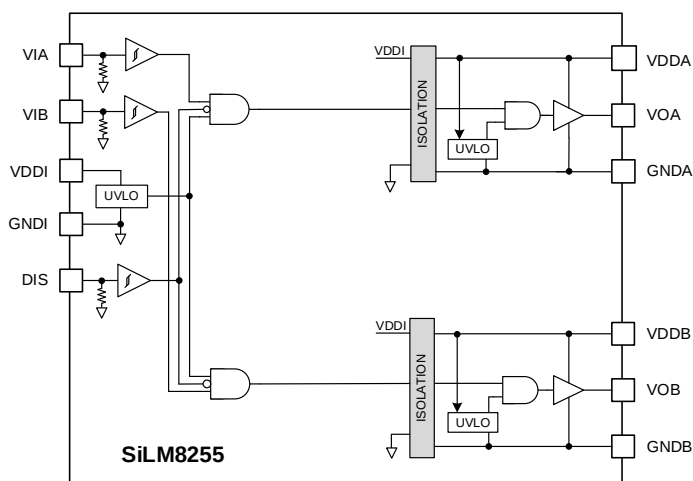


Figure 6. SiLM8255 Functional Block Diagram

ORDERING INFORMATION

Order Part No.	Package	QTY
SiLM8253BDCG-DG	SOP16W, Pb-Free	1500/Reel
SiLM8253DDCG-DG	SOP16W, Pb-Free	1500/Reel
SiLM8254BDCG-DG	SOP16W, Pb-Free	1500/Reel
SiLM8254DDCG-DG	SOP16W, Pb-Free	1500/Reel
SiLM8255BDCG-DG	SOP16W, Pb-Free	1500/Reel
SiLM8255DDCG-DG	SOP16W, Pb-Free	1500/Reel
SiLM8253BDGP-DG	SOP14W, Pb-Free	1500/Reel
SiLM8253DDGP-DG	SOP14W, Pb-Free	1500/Reel
SiLM8254BDGP-DG	SOP14W, Pb-Free	1500/Reel
SiLM8254DDGP-DG	SOP14W, Pb-Free	1500/Reel
SiLM8255BDGP-DG	SOP14W, Pb-Free	1500/Reel
SiLM8255DDGP-DG	SOP14W, Pb-Free	1500/Reel
SiLM8253BBCL-DG	SOP16, Pb-Free	3000/Reel
SiLM8253DBCL-DG	SOP16, Pb-Free	3000/Reel
SiLM8254BBCL-DG	SOP16, Pb-Free	3000/Reel
SiLM8254DBCL-DG	SOP16, Pb-Free	3000/Reel
SiLM8255BBCL-DG	SOP16, Pb-Free	3000/Reel
SiLM8255DBCL-DG	SOP16, Pb-Free	3000/Reel

FAMILY OVERVIEW

Part Number	Input Configuration	Output Configuration	Programmable Dead Time	Overlap Protection	Peak Output Current	UVLO
SiLM8253BDCG-DG SiLM8253BDCEP-DG SiLM8253BBCL-DG	VIA,VIB	HS/LS	Yes	Yes	4.0 A	8.5V/7.5V
SiLM8253DDCG-DG SiLM8253DDCEP-DG SiLM8253DBCL-DG	VIA,VIB	HS/LS	Yes	Yes	4.0 A	12.5V/11.5V
SiLM8254BDCG-DG SiLM8254BDCEP-DG SiLM8254BBCL-DG	PWM	HS/LS	Yes	Yes	4.0 A	8.5V/7.5V
SiLM8254DDCG-DG SiLM8254DDCEP-DG SiLM8254DBCL-DG	PWM	HS/LS	Yes	Yes	4.0 A	12.5V/11.5V
SiLM8255BDCG-DG SiLM8255BDCEP-DG SiLM8255BBCL-DG	VIA,VIB	Dual Driver	No	No	4.0 A	8.5V/7.5V
SiLM8255DDCG-DG SiLM8255DDCEP-DG SiLM8255DBCL-DG	VIA,VIB	Dual Driver	No	No	4.0 A	12.5V/11.5V

ABSOLUTE MAXIMUM RATINGS¹

Symbol	Definition		Min	Max	Unit
V _{DDI}	Input Power Supply Voltage		-0.3	20	V
V _{IA} , V _{IB} , V _{DIS} , V _{PWM}	Input Signal Voltage		-7	20	V
V _{DDA} , V _{DDB}	Driver Power Supply		-0.3	45	V
V _{OUTA} , V _{OUTB}	Driver Output Voltage		-0.3	V _{DDA} +0.3, V _{DDB} +0.3	V
	Driver Output Voltage, Transient for 200ns ²		-3	V _{DDA} +0.3, V _{DDB} +0.3	V
	Driver Output Voltage, Transient for 50ns ²		-6	V _{DDA} +0.3, V _{DDB} +0.3	V
V _{ch2ch}	Channel to Channel Voltage	SOP16W/SOP16		1500	V
		SOP14W		1850	V
T _J	Junction Temperature		-40	150	°C
T _S	Storage Temperature		-65	150	°C

RECOMMENDED OPERATION CONDITIONS¹

Symbol	Definition		Min	Max	Unit
V _{DDI}	Input Power Supply Voltage		3	18	V
V _{IA} , V _{IB} , V _{DIS} , V _{PWM}	Input Signal Voltage		-5	18	V
V _{DDA} , V _{DDB}	Driver Power Supply (8.5V UVLO Version)		9	40	V
V _{DDA} , V _{DDB}	Power Supply for Driver (12.5V UVLO Version)		13.5	40	V
R _{DT}	Resistance range on DT		5	220	kΩ
C _{DT}	Capacitance on DT			10	nF
T _J	Junction Temperature		-40	150	°C
T _A	Storage Temperature		-40	125	°C

ESD RATINGS

Symbol	Definition	Value	Units
V _{ESD}	HBM	±4000	V
	CDM	±2000	

Note 1: V_{DDI}, V_{IA}, V_{IB}, V_{DIS}, V_{PWM} are reference to GNDI; V_{DDA}, V_{OUTA} are referenced to GNDA; V_{DDB}, V_{OUTB} are referenced to GNDB;

Note 2: Values are verified by characterization on bench

THERMAL INFORMATION

Symbol	Definition	Value		Unit
		SOP16W/SOP14W	SOP16	
$R_{\theta JA}$	Junction to ambient thermal resistance	100	150	°C/W
$R_{\theta JC(TOP)}$	Junction to case (top) thermal resistance	40	38	°C/W

PACKAGE SPECIFICATIONS

Symbol	Definition	Min.	Typ.	Max.	Units
R _{IO}	Resistance (Input Side to Output Side)		10 ¹²		Ω
C _{IO}	Capacitance (Input Side to Output Side)		1.8		pF

INSULATION SPECIFICATIONS

Symbol	Definition	Test Condition	Value		Units
			SOP16	SOP16W/ SOP14W	
CLR	External clearance	Shortest terminal to terminal distance through air	>4.0	>8.0	mm
CPG	External creepage	Shortest terminal to terminal distance across the package surface	>4.0	>8.0	mm
DTI	Distance through the insulation	Minimum internal gap	>16	>16	um
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11), IEC 60112	>600	>600	V
	Material Group		I	I	
	Overvoltage category	Rated mains voltages ≤150Vrms	I-IV	I-IV	
		Rated mains voltages ≤300Vrms	I-III	I-IV	
		Rated mains voltages ≤600Vrms	I-II	I-III	
		Rated mains voltages ≤1000Vrms	I-I	I-II	
DIN V VDE 0884-11 ⁽¹⁾					
V _{IORM}	Maximum repetitive peak isolation voltage		1000	1414	V _{PK}
V _{IOWM}	Maximum isolation working voltage		707	1000	V _{RMS}
V _{IOTM}	Maximum transient isolation voltage	60s	4242	7000	V _{PK}
V _{IOSM}	Maximum surge isolation voltage	Test method per IEC62368-1, 1.2/50us waveform, V _{TEST} =1.6 x V _{IOSM} for SOP16W/SOP14W; V _{TEST} =1.3 x V _{IOSM} for SOP16	6000	6250	V _{PK}
q _{pd}	Apparent charge	Method b2: V _{pd(m)} =1.875 x V _{IORM} for SOP16W/SOP14W and V _{pd(m)} =1.5 x V _{IORM} for SOP16, tm=1 s	≤5	≤5	pC
	Climatic Category		40/125/21	40/125/21	
	Pollution Degree		2	2	
UL1577					
V _{ISO}	Withstand Isolation Voltage	V _{TEST} =V _{ISO} , t=60s (qualification), V _{TEST} =1.2 x V _{ISO} , t=1s (100% production)	3000	5000	V _{RMS}

Note 1: Certification planned

SAFETY RELATED CERTIFICATIONS(SOP16W)

VDE	UL	CQC	TUV
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022	Certified according to IEC 61010-1: 2010+A1 and IEC 62368-1: 2020+A11
Reinforced Insulation	Single protection, 5000 V_{RMS}	Reinforced insulation, Altitude $\leq 5000m$, tropical climate	5000Vrms reinforced insulation, 800Vrms maximum working voltage
Pending	File number: E521801	File number: CQC23001379622	Ref.Certif.No: DE 2-038921-M1 Ref.Certif.No: JPTUV-146634-M1 Re Certif.No: R 50590519

SAFETY LIMITING VALUES (SOP16W)

Symbol	Parameter	Condition	Side	Value	Unit
I_s	Safety output current	$V_{DDA}=V_{DDB}=16V$, $R_{\theta JA}=100^{\circ}C/W$, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$	Driver A and Driver B	73	mA
P_s	Safety input, output, or total power	$V_{DDA}=V_{DDB}=16V$, $R_{\theta JA}=100^{\circ}C/W$, $T_J = 150^{\circ}C$, $T_A = 25^{\circ}C$	Input	36	mW
			Driver A	584	
			Driver B	584	
			Total	1204	
T_s	Maximum safety temperature			150	$^{\circ}C$

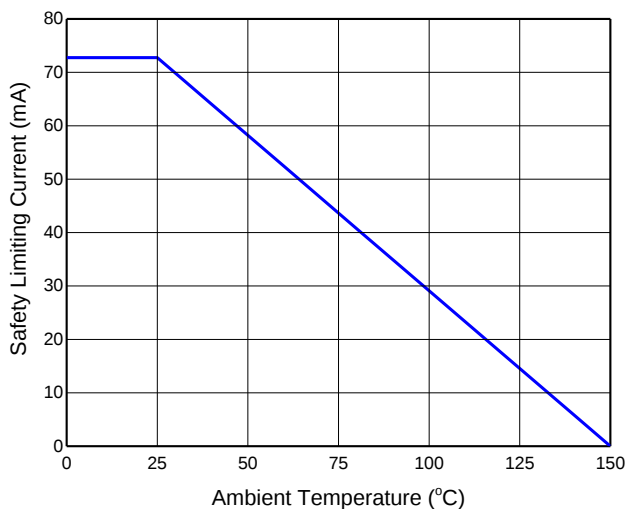


Figure 7. Thermal Derating Curve for Limiting Current per VDE (Current in VDDA and VDDB), SOP16W

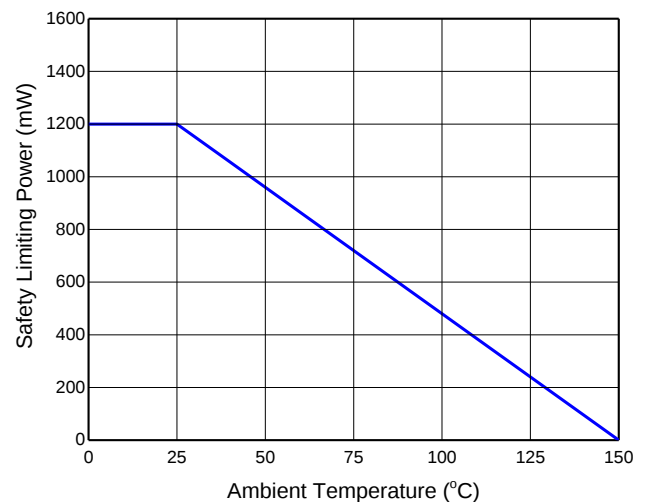


Figure 8. Thermal Derating Curve for Limiting Power per VDE, SOP16W

SAFETY RELATED CERTIFICATIONS(SOP16)

VDE	UL	CQC
DIN VDE 0884-17: 2021-10	UL 1577 component recognition program	Certified according to GB4943.1-2022
Basic Insulation	Single protection, 3000 V _{RMS}	Basic insulation, Altitude ≤ 5000m, Tropical climate
Pending	File number: E521801	File number: CQC23001379622

SAFETY LIMITING VALUES (SOP16)

Symbol	Parameter	Condition	Side	Value	Unit
I _s	Safety output current	V _{DDA} =V _{ddb} =16V, R _{θJA} =150°C/W, T _J =150°C, T _A =25°C	Driver A and Driver B	49.8	mA
P _s	Safety input, output, or total power	V _{DDA} =V _{ddb} =16V, R _{θJA} =150°C/W, T _J =150°C, T _A =25°C	Input	36	mW
			Driver A	399	
			Driver B	399	
			Total	834	
T _s	Maximum safety temperature			150	°C

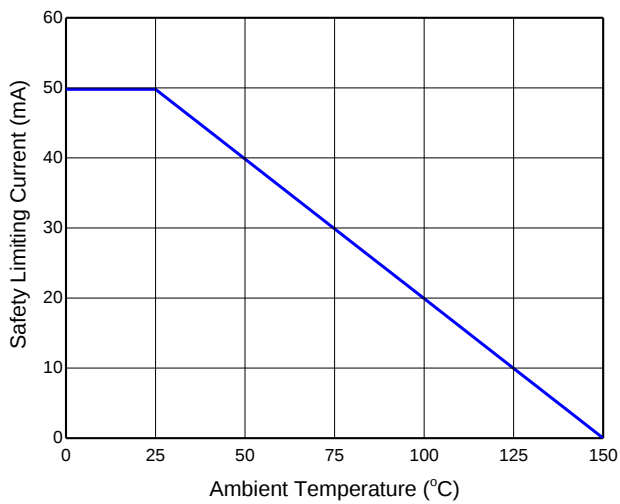


Figure 9. Thermal Derating Curve for Limiting Current per VDE (Current in VDDA and Vddb), SOP16

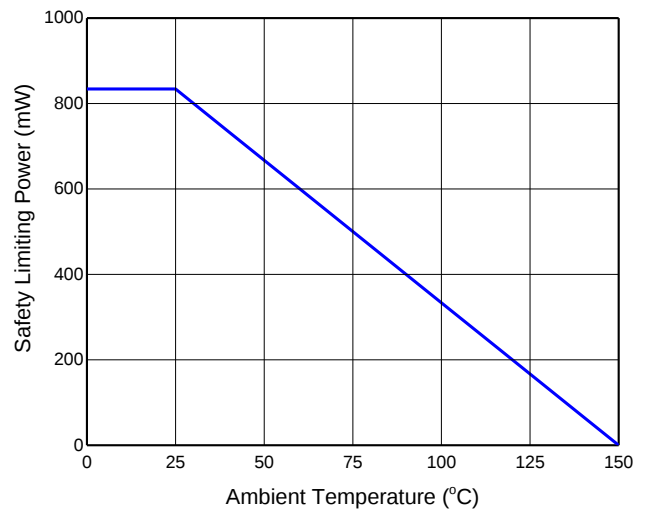


Figure 10. Thermal Derating Curve for Limiting Power per VDE, SOP16

ELECTRICAL CHARACTERISTICS (DC)

$V_{DDI} = 5\text{ V}$, $0.1\mu\text{F}$ capacitor from V_{DDI} to $GNDI$, $V_{DDA} = V_{ddb} = 15\text{V}$, $1\mu\text{F}$ capacitor from V_{DDA} and V_{ddb} to $GND A$ and $GND B$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Input Power Supply						
V_{DDI}	Input Supply Voltage		3		18	V
$V_{UVLO_VDDI_R}$	VDDI UVLO Rising		2.5	2.7	2.9	V
$V_{UVLO_VDDI_F}$	VDDI UVLO Falling		2.3	2.5	2.7	V
V_{UVLO_HYS}	VDDI UVLO Hysteresis			0.2		V
I_{VDDI}	Quiescent Current	$V_{IA} = 0\text{V}$, $V_{IB} = 0\text{V}$	1.4	2	2.6	mA
	Operation Current	$f_{sw} = 50\text{kHz}$, (50% Duty Cycle), both channels	1.9	2.5	3.1	mA
Logic Interface						
V_{IH}	High Level Input Threshold Voltage at V_{IA} , V_{IB} , DIS and PWM			1.7	2.1	V
V_{IL}	Low Level Input Threshold Voltage at V_{IA} , V_{IB} , DIS and PWM		0.8	1.1		V
R_{PD}	Pull down Resistance on V_{IA} , V_{IB} , DIS and PWM		100	170	280	k Ω
Driver Power Supply						
$V_{UVLO_VDDA_R}$, $V_{UVLO_Vddb_R}$	VDDA, Vddb UVLO Rising	8.5V UVLO Version	8	8.5	9	V
		12.5V UVLO Version	11.5	12.5	13.5	V
$V_{UVLO_VDDA_F}$, $V_{UVLO_Vddb_F}$	VDDA, Vddb UVLO Falling	8.5V UVLO Version	7	7.5	8	V
		12.5V UVLO Version	10.5	11.5	12.5	V
$V_{UVLO_VDDA_HYS}$, $V_{UVLO_Vddb_HYS}$	VDDA, Vddb UVLO Hysteresis	8.5V UVLO Version		1		V
		12.5V UVLO Version		1		V
I_{VDDA} , I_{Vddb}	VDDA/B Quiescent Current, per Channel	$V_{IA} = 0\text{V}$, $V_{IB} = 0\text{V}$	0.8	1.5	2.6	mA
OUTPUT						
I_{OH}	Peak Source Current			4		A
I_{OL}	Peak Sink Current			7		A
V_{OH}	High Level Output Voltage	$I_O = -10\text{mA}$		12	22	mV
V_{OL}	Low Level Output Voltage	$I_O = 10\text{mA}$		6.2	11	mV
Dead Time						
t_{DT}	Dead time	$R_{DT} = 20\text{k}\Omega$	160	200	240	ns

SWITCHING CHARACTERISTICS (AC)

$V_{DDI} = 5\text{ V}$, $0.1\mu\text{F}$ capacitor from V_{DDI} to $GNDI$, $V_{DDA} = V_{DDB} = 15\text{ V}$, $1\mu\text{F}$ capacitor from V_{DDA} and V_{DDB} to $GNDA$ and $GNDB$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Switching Characteristics						
t_{PLH}	Propagation Delay, Low to High	$C_{LOAD}=1\text{ nF}$, $f_{SW}=1\text{ kHz}$, (50% Duty Cycle)		40	60	ns
t_{PHL}	Propagation Delay, High to Low			40	60	ns
t_r	Turn on Rise Time			6	15	ns
t_f	Turn off Fall Time			4	10	ns
t_{PWD}	Pulse Width Distortion				18	ns
t_{DM}	Propagation Delay Matching between OUTA and OUTB				18	ns
$t_{UVLO_REC_VDDI}$	VDDI UVLO Recovery Delay			15		μs
$t_{UVLO_REC_VDDA(B)}$	VDDA, VDDB UVLO Recovery Delay			18		μs
$CMTI_H$	High Level Static Common Mode Transient Immunity	$V_{CM}=1000\text{ V}$, $T_A=25^\circ\text{C}$	100			$\text{kV}/\mu\text{s}$
$CMTI_L$	Low Level Static Common Mode Transient Immunity	$V_{CM}=1000\text{ V}$, $T_A=25^\circ\text{C}$	100			$\text{kV}/\mu\text{s}$

PARAMETER MEASUREMENT INFORMATION

Propagation Delay and Pulse Width Distortion

Figure 11 shows the timing diagram of the propagation delay t_{PLH} and t_{PHL} , pulse distortion t_{PWD} and delay matching t_{DM} from the input V_{IA} and V_{IB} .

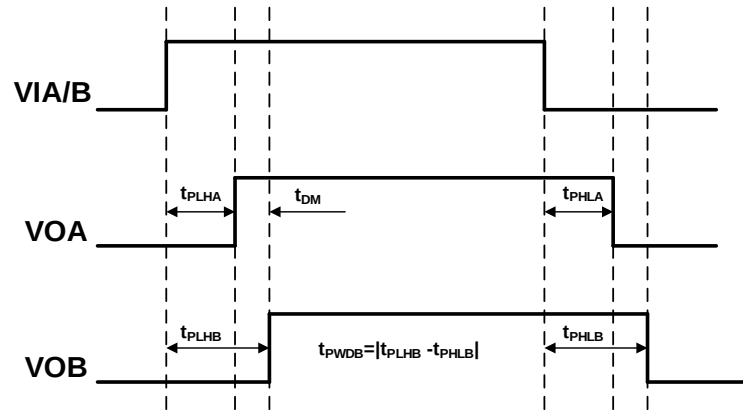


Figure 11. Propagation Delay and Pulse Width Distortion

Rise and Fall Time Testing

Figure 12 shows the criteria for measuring rise time (t_r) and fall time (t_f).

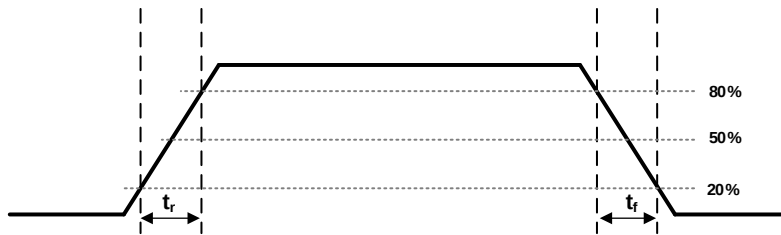


Figure 12. Turn On Rise Time and Turn Off Fall Time

CMTI Testing

Figure 13 is the simplified diagram of the CMTI testing. Common mode voltage is set to 1000V.

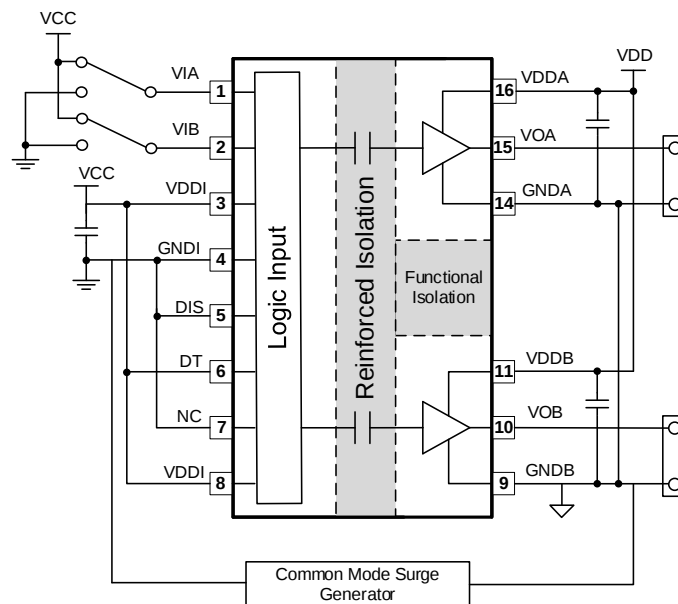


Figure 13. CMTI Test Circuit

FEATURE DESCRIPTION

SiLM825x is a flexible dual channel isolated gate driver that can drive IGBTs and MOSFETs. It has 4.0A peak output current capability with maxim output driver supply voltage of 40V. SiLM825x has many features that allow it to integrate well with control circuitry and protect the gates it drives such as: resistor programmable dead time control, an DIS pin, and under voltage lock out (UVLO) for both input and output voltages.

Under Voltage Lockout

The SiLM825x has under voltage lock out (UVLO) protection feature on each driver power supply voltage between the VDDA (VDDDB) and GNDA (GNDB) pins. When the VDDx voltage is lower than $V_{UVLO_VDDX_R}$, during device start up or lower than $V_{UVLO_VDDX_F}$, after start up, the VDDA (VDDDB) UVLO feature holds the driver output low, regardless of the status of the input pins. A hysteresis on the UVLO feature prevents glitch when there is noise from the power supply.

The SiLM825x also monitors the input power supply and there is an internal under voltage lock out protection feature on the VDDI. The driver outputs (VOA and VOB) are hold low when the voltage on the VDDI is lower than $V_{UVLO_VDDI_R}$ during start up or lower than $V_{UVLO_VDDI_F}$ after start up. There is a hysteresis on the VDDI UVLO feature to prevent glitch due the noise on the VDDI power supply.

Disable Input Function

When the DIS is pulled high, the VOA and VOB are pulled low regardless of the states of VIA and VIB. When the DIS pin is pulled low, the VOA and VOB are allowed for normal operation and controlled by the VIA and VIB.

The DIS input has no effect if VDDI is below its UVLO threshold and VOA, VOB remain low. There is an internal pull down resistor on the DIS pin.

Control Input and Output Logic

The VIA and VIB input controls the corresponding output channel, VOA and VOB. A logic high signal on VIA (VIB) causes the output of VOA (VOB) to go high. And a logic low on VIA (VIB) causes the output of VOA (VOB) to go low.

For PWM input versions (SiLM8254), when the PWM input is high, the VOA is high and VOB is low. And when the PWM input is low, the VOA is low and VOB is high.

The Table 4 and Table 5 show the relationship between VIA, VIB, PWM, DIS, UVLO and Output of VOA and VOB.

Table 4. Relationship between Input and Output with VIA, VIB input (SiLM8253/5)

VIA	VIB	DIS	VDDI UVLO	VDDA UVLO	VDDB UVLO	VOA	VOB	Note
H	L	L	No	No	No	H	L	
L	H	L	No	No	No	L	H	
L	L	L	No	No	No	L	L	
H	H	L	No	No	No	H	H	SiLM8255
						L	L	SiLM8253
X	X	H	No	No	No	L	L	Device disabled
X	X	X	Yes	No	No	L	L	VDDI UVLO active
H	X	L	No	No	Yes	H	L	VDDB UVLO active
L	X	L	No	No	Yes	L	L	
X	H	L	No	Yes	No	L	H	VDDA UVLO active
X	L	L	No	Yes	No	L	L	

Table 5. Relationship between Input and Output with PWM input (SiLM8254)

PWM	DIS	VDDI UVLO	VDDA UVLO	VDDB UVLO	VOA	VOB	Note
H	L	No	No	No	H	L	
L	L	No	No	No	L	H	
X	H	No	No	No	L	L	Device disabled
X	X	Yes	No	No	L	L	VDDI UVLO active
H	L	No	No	Yes	H	L	VDDDB UVLO active
L	L	No	No	Yes	L	L	
H	L	No	Yes	No	L	L	VDDA UVLO active
L	L	No	Yes	No	L	H	

Dead-time Program

For the high side/low side configuration driver, there is a dead-time between VOA and VOB. The dead-time delay (t_{DT}) is programmed by a resistor (R_{DT}) connected from the DT input to ground and it can be calculated with below equation.

$$t_{DT}[\text{ns}] \approx 10 \times R_{DT}[\text{k}\Omega]$$

Here, t_{DT} is the dead-time delay, R_{DT} is the resistance value between DT and ground.

The DT pin can be connected to VDDI or left floating to provide a nominal dead time at approximately 400 ps.

A bypassing capacitor, 2.2nF or greater, is recommended to be put between DT and GNDI to achieve better noise immunity.

The Figure 14 shows the input and output logic with dead-time in different condition.

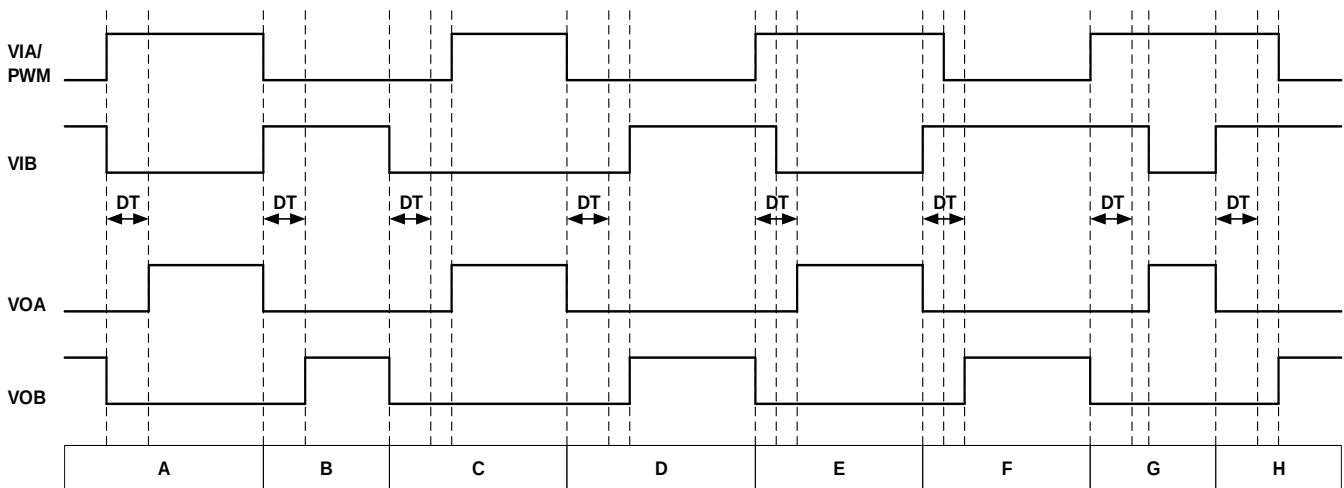


Figure 14. Input and output logic with dead-time

Condition A: VIA goes high and VIB goes low. VOB goes low immediately and VOA goes high after the programmed dead-time.

Condition B: VIA goes low and VIB goes high. VOA goes low immediately and VOB goes high after the programmed dead-time.

Condition C: VIB goes low and VIA still low. VOB goes low immediately. Since the VIA input dead-time is longer than the programmed dead-time, the VOA goes high immediately when the VIA input goes high.

Condition D: VIA goes low and VIB still low. VOA goes low immediately. Since the VIB input dead-time is longer than the programmed dead-time, the VOB goes high immediately when the VIB input goes high.

Condition E: VIA goes high while VIB and VOB are still high, the overlap time is shorter than the programmed dead-time. To avoid overshoot, VOB goes low immediately when the VIA goes high. The VOA goes high after the programmed dead-time.

Condition F: VIB goes high while VIA and VOA are still high, the overlap time is shorter than the programmed dead-time. To avoid overshoot, VOA goes low immediately when the VIB goes high. The VOB goes high after the programmed dead-time.

Condition G: VIA goes high while VIB and VOB are still high, the overlap time is longer than the programmed dead-time. To avoid overshoot, VOB goes low immediately when the VIA goes high. Since the overlap time is longer than the programmed dead-time, the VOA goes high immediately when the VIB goes low.

Condition H: VIB goes high while VIA and VOA are still high, the overlap time is longer than the programmed dead-time. To avoid overshoot, VOA goes low immediately when the VIB goes high. Since the overlap time is longer than the programmed dead-time, the VOB goes high when the VIA goes low.

APPLICATION INFORMATION

The circuit in Figure 15 shows the typical application circuit for SiLM825x to driver a typical half bridge configuration which could be used in several popular power converter topologies such as synchronous buck, synchronous boost, half bridge, full bridge, LLC etc. topologies and 3-phase motor drive applications.

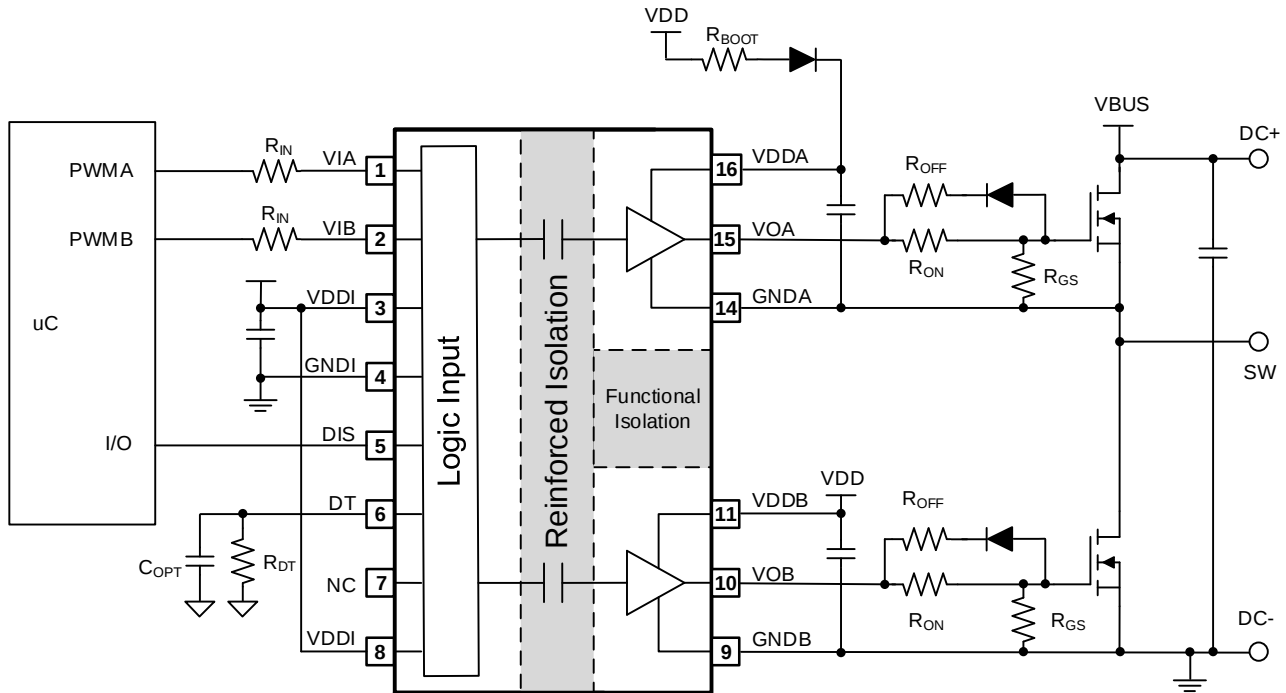


Figure 15. Typical Application Schematic

PACKAGE CASE OUTLINES

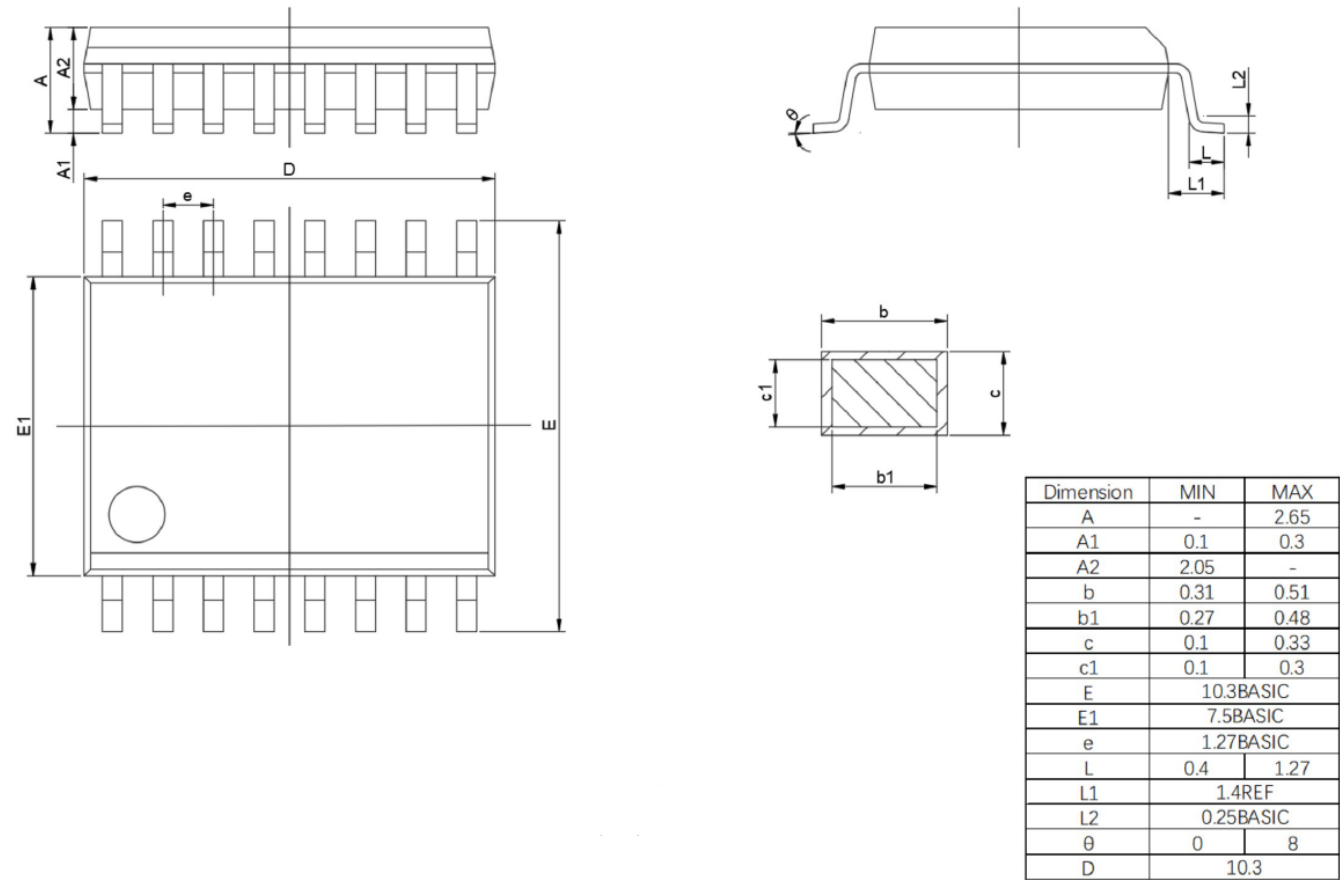


Figure 16. SOP16W Package Outline Dimensions

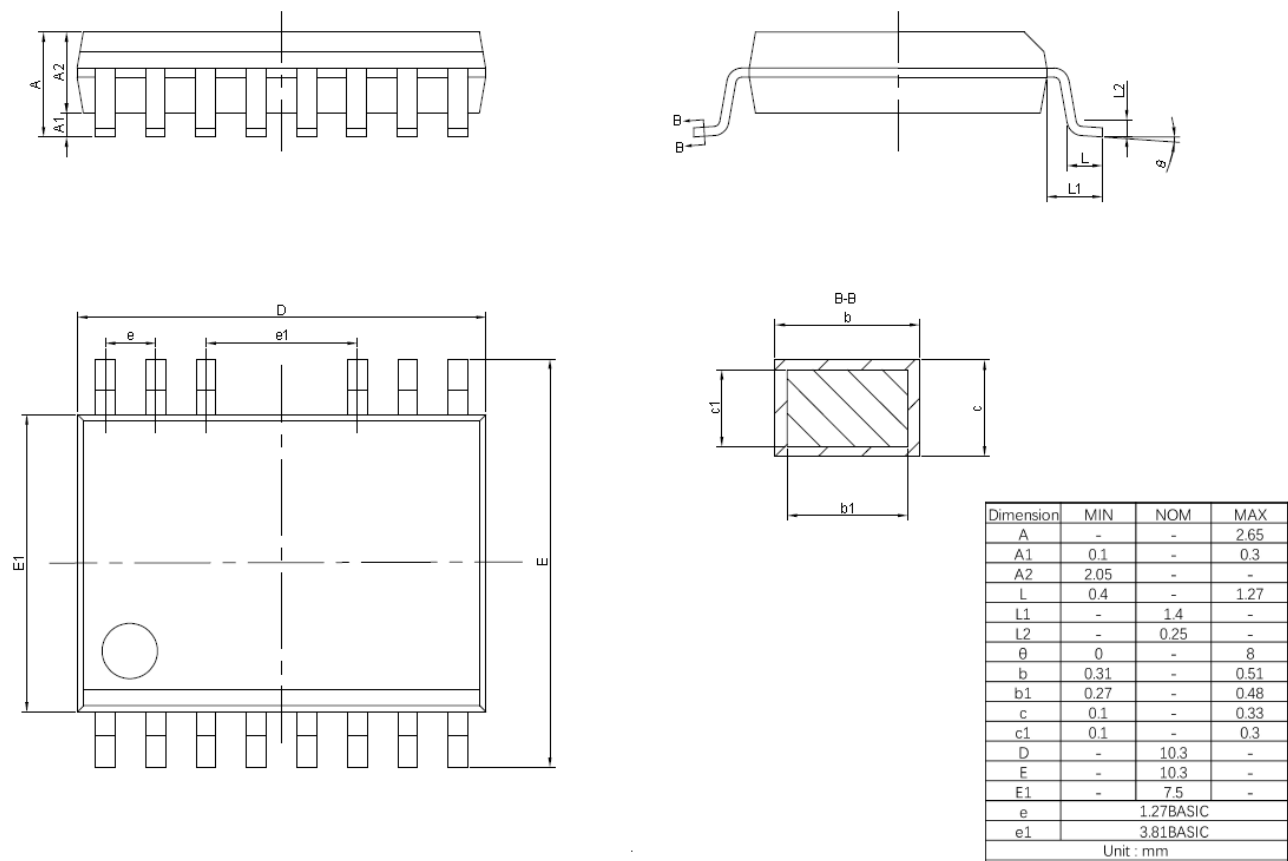


Figure 17. SOP14W Package Outline Dimensions

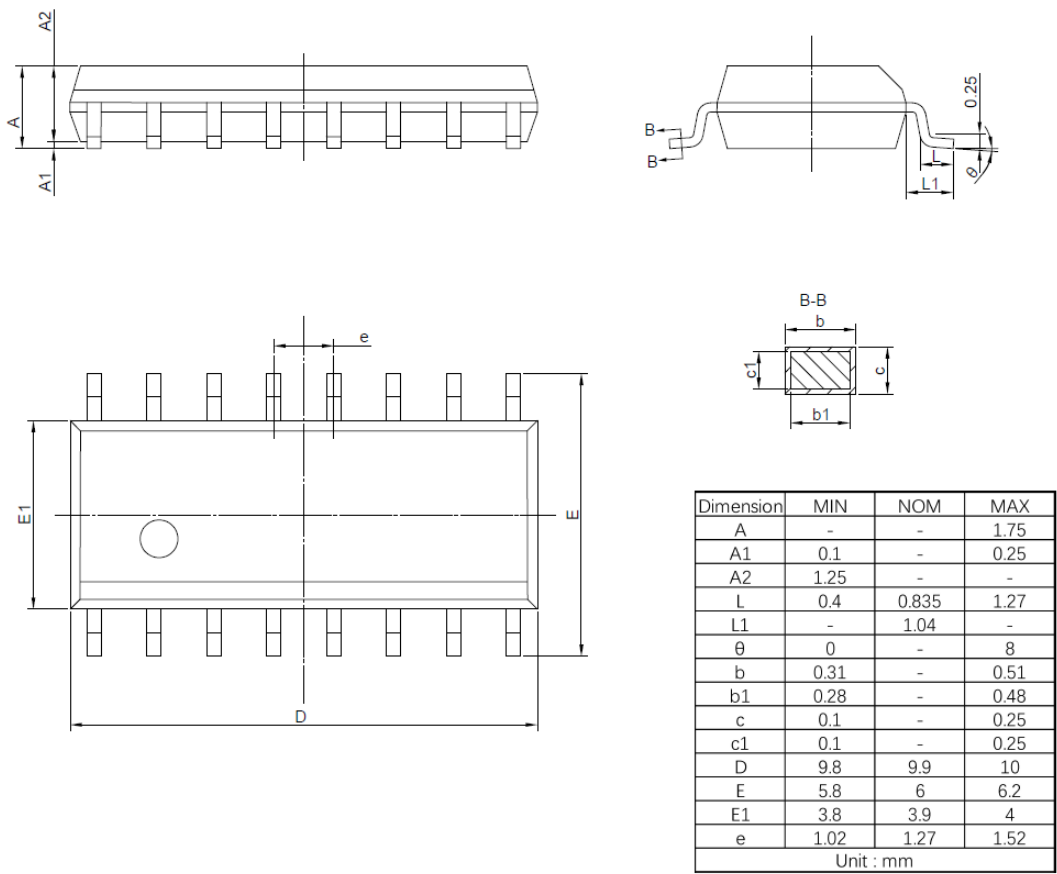
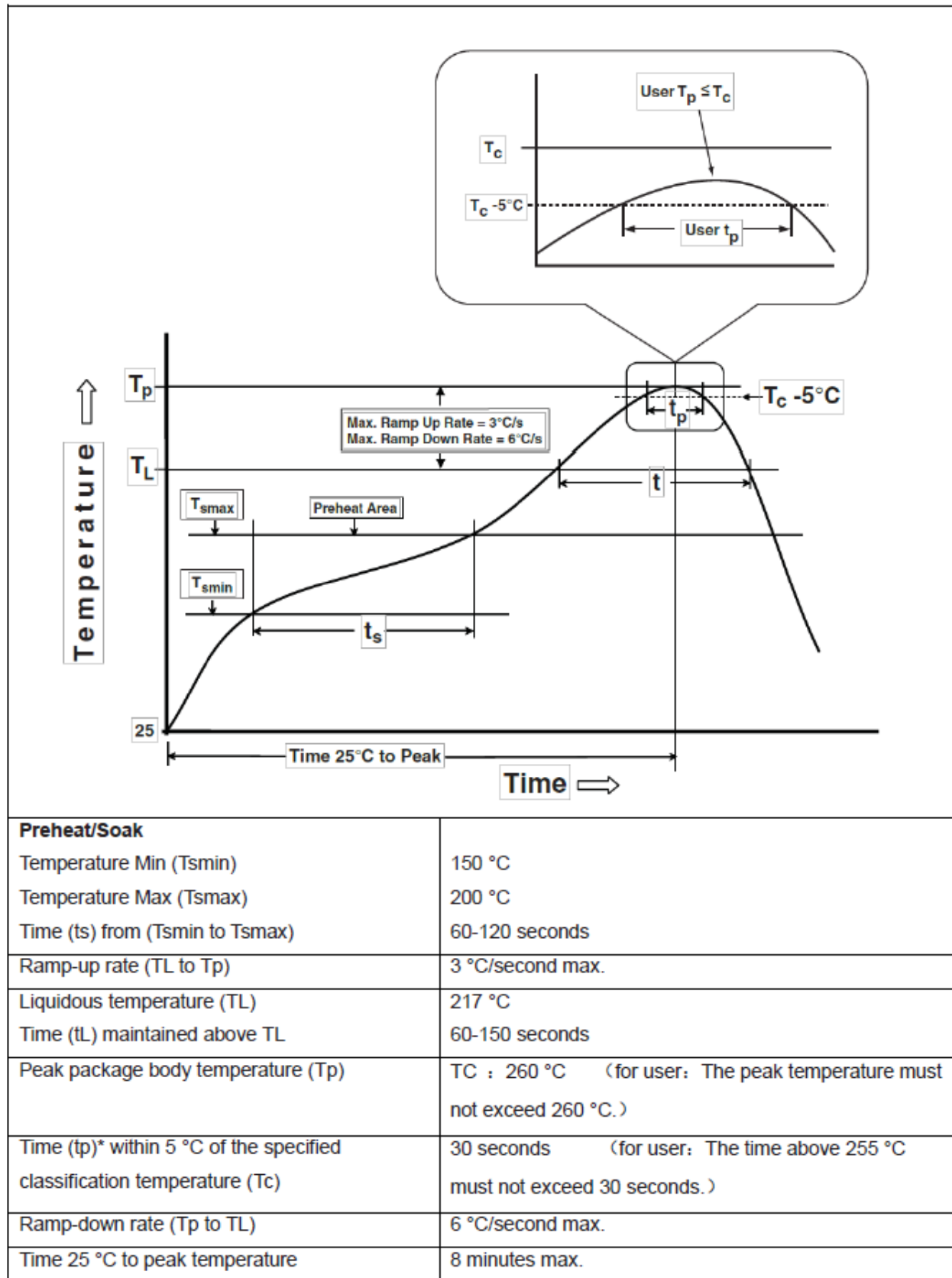


Figure 18. SOP16 Package Outline Dimensions

REFLOW PROFILE GUIDANCE



REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet: 2024-05-20	
Whole document	Initial datasheet release
Rev 1.1 datasheet: 2025-03-20	
Page 13	Add TUV certification